CLAIMS

1. A photodetector circuit including a photodiode detector (312/314) and an associated readout circuit, characterised in that the circuit incorporates a CMOS component (300 to 312), at least one epitaxial layer (314) which is an active region of the photodiode detector and a guard ring (310) delimiting the photodiode detector (312/314) to enhance electric field uniformity and inhibit breakdown.

2. A photodetector circuit according to Claim 1 characterised in that the CMOS component comprises a substrate (600) supporting and insulated from CMOS circuitry (606), the photodiode detector (600/614/616/620) is operable in current multiplication mode and the at least one epitaxial layer (616) is deposited upon the substrate (600).

3. A photodetector circuit according to Claim 2 characterised in that the photodiode detector is a PIN structure (600/614/616/620) in which the at least one epitaxial layer (616) provides a high field region.

4. A photodetector circuit according to Claim 2 characterised in that the photodiode detector is an avalanche photodiode (600/614/616/620) and comprises a first region (614) incorporated in the substrate (600), and the at least one epitaxial layer is a layer (616) upon the first region (614) and provides a second region of the photodiode.

5. A photodetector circuit according to Claim 2 characterised in that the at least one epitaxial layer comprises two layers (616, 620) providing second and third regions of the photodiode (600/614/616/620), the second region (616) is upon the first region (614) and the third region (620) is upon the second region (616), the first and third regions (614, 620) are of mutually opposite conductivity type, the second region (616) is substantially undoped and the third region (620) is an epitaxial layer.

6. A photodetector circuit according to Claim 5 characterised in that the third

avalanche photodiode region (620) is electrically connected to the guard ring (612) and has like potential therewith during circuit operation

7. A photodetector circuit according to Claim 1 characterised in that it is arranged to provide a logarithmic response to incident radiation.

8. A photodetector circuit according to Claim 1 characterised in that it incorporates parasitic photodiodes (PPD21, PPD22) arranged to contribute to circuit output in response to incident radiation.

9. A photodetector circuit according to Claim 1 characterised in that it includes an amplifier (MA51/MA52) arranged to provide feedback to stabilise photodiode detector bias voltage.

10. A photodetector circuit according to Claim 9 characterised in that the amplifier (MA51/MA52) is arranged to amplify an output signal from the photodiode detector (APD5) and to provide feedback to bias a load transistor (ML5) in series with the photodiode detector (APD5).

11. A photodetector circuit according to Claim 10 characterised in that the amplifier is a push-pull amplifier (MA71/MA72).

12. A photodetector circuit according to Claim 10 characterised in that it includes a cascode transistor (MC9) arranged to reduce Miller Effect capacitance in the amplifier (MA91/MA92).

13. A photodetector circuit according to Claim 1 characterised in that the CMOS component is a substrate (600) supporting and insulated from CMOS circuitry (606), the photodiode detector comprises a first region of one conductivity type (614) incorporated in the substrate, the at least one epitaxial layer comprises two epitaxial layers (616, 620) one of which (616) is substantially undoped and the other of which (620) is of opposite conductivity type to that of the first region (614), the first region (614) and the two epitaxial layers (616, 620) being configured as a PIN diode.

14. A photodetector circuit according to Claim 13 characterised in that the undoped epitaxial layer is of SiGe alloy or is a quantum well structure of the $Si_{1-x}Ge_x$ material system where the value of the compositional parameter x changes between successive layers.

15. A photodetector circuit including a photodiode detector and an associated readout circuit, characterised in that it is arranged to provide a logarithmic response to incident radiation and incorporates at least one silicon-germanium alloy region (261, 278) arranged for photon absorption to which the circuit is responsive, such region being in at least one of the photodiode detector and a substrate supporting the circuit.

16. A photodetector circuit according to Claim 15 characterised in that it incorporates parasitic photodiodes arranged to contribute to circuit output in response to incident radiation.

17. A photodetector circuit according to Claim 15 characterised in that the photodiode detector is an avalanche photodiode (260).

18. A photodetector circuit according to Claim 15 characterised in that it includes an amplifier (MA51/MA52) arranged to provide feedback to stabilise photodiode detector bias voltage.

19. A photodetector circuit according to Claim 15 characterised in that the amplifier (MA51/MA52) is arranged to amplify an output signal from the photodiode detector (APD5) and to provide feedback to bias a load transistor (ML5) in series with the photodiode detector (APD5).

20. A photodetector circuit according to Claim 19 characterised in that the amplifier (MA91/MA92) includes a cascode transistor (MC9) arranged to reduce Miller Effect capacitance.

21. A photodetector circuit according to Claim 15 characterised in that the amplifier is a push-pull amplifier (MA81/MA82).

22. An array of photodetector pixel circuits each including an avalanche photodiode detector (APD5) and an associated readout circuit (50), characterised in that each readout circuit (50) includes an amplifier (MA51/MA52) arranged to provide feedback to a transistor load (ML5) in series with the detector (APD5) to stabilise photodiode detector bias voltage and to provide an output indicating radiation intensity illuminating the detector (APD5), and each readout circuit (50) is implemented by circuit elements integrated within the respective pixel circuit.

23. An array according to Claim 22 characterised in that each avalanche photodiode detector (600/614/616/620) comprises epitaxial semiconductor material (616) upon a substrate (600), and the amplifier is incorporated in CMOS circuitry (606) supported by the substrate (600) but insulated from it.

24. An array according to Claim 23 characterised in that the epitaxial semiconductor material comprises two epitaxial layers (616, 620) which in combination with the substrate (600/612) provide a PIN diode structure.

25. An array according to Claim 23 characterised in that for each photodetector pixel circuit the substrate (600) has an in-diffusion of dopant material providing one region (614) of the associated avalanche photodiode detector (600/614/616/620).

26. An array according to Claim 22 characterised in that each avalanche photodiode detector (600/614/616/620) is operable in a current multiplication sub-Geiger mode at low incident radiation intensities and in a non-multiplication mode at high incident radiation intensities.

27. An array according to Claim 22 characterised in that it incorporates parasitic photodiodes (PPD21, PPD22) connected in parallel with the avalanche photodiode detector (APD1) and arranged to contribute to circuit output in response to incident radiation.

28. An array according to Claim 22 characterised in that each pixel circuit amplifier (MA91/MA92) includes a respective cascode transistor (MC9) arranged to reduce

Miller Effect capacitance.

29. A photodetector circuit according to Claim 22 characterised in that each pixel circuit amplifier is a push-pull amplifier (MA81/MA82).

30. A method of making a photodetector circuit incorporating a photodiode detector (600/614/616/620) and an associated readout circuit (606), the method including the step of producing a CMOS circuit component (600/602/606), characterised in that the method also includes producing upon the CMOS circuit component (600/602/606) at least one epitaxial layer (616) providing an active region of the photodiode detector (600/614/616/620) and a guard ring (612) delimiting the photodiode detector to enhance electric field uniformity and inhibit breakdown.

31. A method according to Claim 30 characterised in that it includes the step of forming a first region (614) of one conductivity type within the guard ring (612), and wherein the step of producing the at least one epitaxial layer comprises producing upon the first region (614) a epitaxial layer (616) , the photodiode detector (600/614/616/620) being delimited by the guard ring (612) in order substantially to avoid corners and related features associated with undesirable localised enhancement of electric field.

32. A method according to Claim 31 characterised in that the epitaxial layer (616) is surmounted by a layer (620) of opposite conductivity type to the first region (614).

33. A method according to Claim 31 characterised in that it includes the step of producing a first region (614) of one conductivity type incorporated in the CMOS component (600/602/606), and wherein the step of producing the at least one epitaxial layer comprises producing two epitaxial layers (616, 620) one of which (616) is substantially undoped and the other of which (620) is of opposite conductivity type to that of the first region (614) to provide a PIN avalanche photodiode.

34. A method according to Claim 33 characterised in that the undoped epitaxial layer (616) is of SiGe alloy or is a quantum well structure of the $Si_{1-x}Ge_x$ material

system where the value of the compositional parameter x changes between successive layers.

35. A method of making a photodetector circuit incorporating a photodiode detector (600/614/616/620) and an associated readout circuit (606), the method including the step of producing a CMOS circuit component (600 to 606), characterised in that the CMOS circuit component is a substrate (600) bearing an insulating region (602) itself supporting the readout circuit (606), the readout circuit (606) is a CMOS structure, and the method includes producing upon the substrate (600):

a) at least one epitaxial layer (616) providing an active region of the photodiode detector (600/614/616/620), and

b) a guard ring (612) delimiting the photodiode detector to enhance electric field uniformity and inhibit breakdown.

36. A method according to Claim 35 characterised in that the at least one epitaxial layer is an epitaxial layer (616) which is substantially undoped and is a central high field region of the photodiode detector (600/614/616/620) between two other such regions (614, 620), the other regions (614, 620) being of mutually opposite conductivity type.

37. A method according to Claim 38 characterised in that one of the other regions (614, 620) is a doped region (614) of the substrate (600).